APPENDIX C

(CLEAN VERSION OF CLAIMS)

(Serial No. 09/652,495)

CLAIMS

What is claimed is:

1. A chip-scale package, comprising:

a semiconductor device including an active surface; and

a semiconductor substrate disposed adjacent said active surface and including at least one electrically conductive via therethrough and in communication with a corresponding bond pad of said semiconductor device.

2. The chip-scale package of claim 1, further comprising an electrically conductive bump protruding from said semiconductor substrate opposite said semiconductor device and in communication with said at least one electrically conductive via.

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3. (Amended) The chip-scale package of claim 1, wherein said at least one electrically conductive via extends substantially directly through said semiconductor substrate.

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4. (Amended) The chip-scale package of claim 1, further comprising a substantially laterally extending conductive trace in communication with said at least one electrically conductive via.

5. The chip-scale package of claim 1, wherein a substrate of said semiconductor device and said semiconductor substrate comprise the same material.

6. The chip-scale package of claim 1, wherein a substrate of said semiconductor device and said semiconductor substrate comprise materials having substantially the same coefficients of thermal expansion.

7. The chip-scale package of claim 1, wherein a substrate of said semiconductor device comprises silicon.

8. The chip-scale package of claim 1, wherein said semiconductor substrate comprises silicon.

9. The chip-scale package of claim 1, wherein a first thickness of said semiconductor device and a second thickness of said semiconductor substrate are substantially the same.

10. The chip-scale package of claim 1, wherein a first thickness of said semiconductor device is greater than a second thickness of said semiconductor substrate.

11. The chip-scale package of claim 1, wherein a surface of said semiconductor substrate located opposite said semiconductor device comprises an insulative material.

12. The chip-scale package of claim 11, wherein said insulative material comprises a layer extending substantially over said surface.

13. The chip-scale package of claim 11, wherein said insulative material comprises an oxide.

14. The chip-scale package of claim 11, wherein said insulative material comprises silicon oxide.

15. The chip-scale package of claim 1, further comprising an intermediate layer disposed between said semiconductor device and said semiconductor substrate.

16. The chip-scale package of claim 15, wherein said intermediate layer comprises an adhesive material.

17. The chip-scale package of claim 15, wherein said intermediate layer comprises polyimide.

18. The chip-scale package of claim 15, wherein said at least one electrically conductive via and said corresponding bond pad communicate through said intermediate layer.

19. The chip-scale package of claim 1, wherein conductive material of said at least one electrically conductive via is bonded to said corresponding bond pad.

20. The chip-scale package of claim 1, wherein a contact between said at least one electrically conductive via and said corresponding bond pad comprises a diffusion region comprising a bond pad material and a via material.

21. The chip-scale package, comprising:

a semiconductor substrate; and

a semiconductor device invertedly disposed adjacent said semiconductor substrate so that at least one bond pad of said semiconductor device communicates through a corresponding via of said semiconductor substrate.

22. The chip-scale package of claim 21, wherein said at least one bond pad contacts said corresponding via.

23. The chip-scale package of claim 22, further comprising a diffusion region between said at least one bond pad and said corresponding via.

24. The chip-scale package of claim 23, wherein said diffusion region comprises a bond pad material and a via material.

25. The chip-scale package of claim 24, wherein said diffusion region at least partially secures said semiconductor device to said semiconductor substrate.

26. The chip-scale package of claim 21, further comprising an intermediate layer disposed between said semiconductor substrate and said semiconductor device.

27. The chip-scale package of claim 26, wherein said at least one bond pad and said corresponding via contact each other through said intermediate layer.

28. The chip-scale package of claim 26, wherein said intermediate layer comprises a material which adheres said semiconductor device to said semiconductor substrate.

29. The chip-scale package of claim 26, wherein said intermediate layer comprises a polyimide.

30. The chip-scale package of claim 21, further comprising a conductive bump in communication with said corresponding via and protruding from said semiconductor substrate opposite said semiconductor device.

31. The chip-scale package of claim 30, wherein said conductive bump comprises solder.

32. The chip-scale package of claim 21, wherein said semiconductor substrate and a substrate of said semiconductor device comprise the same material.

33. The chip-scale package of claim 21, wherein said semiconductor substrate comprises silicon.

34. The chip-scale package of claim 21, wherein a substrate of said semiconductor device comprises silicon.

35. The chip-scale package of claim 21, wherein a first thickness of said semiconductor substrate and a second thickness of said semiconductor device are substantially equal.

36. The chip-scale package of claim 21, wherein a first thickness of said semiconductor substrate is less than a second thickness of said semiconductor device.

37. The chip-scale package of claim 21, further comprising an insulative material disposed on a surface of said semiconductor substrate opposite said semiconductor device.

38. The chip-scale package of claim 37, wherein said corresponding via is exposed through said insulative material.

39. The chip-scale package of claim 37, wherein said insulative material comprises an oxide.

40. The chip-scale package of claim 37, wherein said insulative material comprises silicon oxide.

41. The chip-scale package of claim 37, wherein said insulative material comprises an insulative layer disposed substantially over said surface.

42. (Amended) The chip-scale package of claim 21, further comprising a conductive trace extending substantially laterally from said corresponding via.

43. (Amended) A flip-chip carrier, comprising a semiconductor substrate including at least one via formed therethrough and positioned to substantially align with a corresponding bond pad of a semiconductor device to be assembled with said semiconductor substrate.

44. The flip-chip carrier of claim 43, wherein said at least one via comprises an electrically conductive material.

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45. The flip-chip carrier of claim 43, further comprising an insulative material disposed on at least one surface of said semiconductor substrate.

46. The flip-chip carrier of claim 45, wherein said insulative material comprises an oxide.

47. The flip-chip carrier of claim 45, wherein said insulative material comprises silicon oxide.

48. The flip-chip carrier of claim 45, wherein said insulative material comprises an insulative layer disposed substantially over said at least one surface.

49. The flip-chip carrier of claim 45, wherein said at least one via is exposed through said insulative material.

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50. The flip-chip carrier of claim 43, wherein said semiconductor substrate comprises silicon.

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51. (Amended) The flip-chip carrier of claim 43, further comprising a conductive bump disposed adjacent an end of said at least one via.

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52. The flip-chip carrier of claim 51, wherein said conductive bump comprises solder.

53. The flip-chip carrier of claim 43, further comprising an adhesive layer disposed adjacent a surface of said semiconductor substrate.

54. The flip-chip carrier of claim 53, wherein said adhesive layer comprises a polyimide.

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55. The flip-chip carrier of claim 53, wherein an end of said at least one via extends through said adhesive layer.

56. The flip-chip carrier of claim 43, further comprising a conductive trace extending substantially laterally from said at least one via.

57. A method of fabricating a chip-scale package, comprising:
defining at least one aperture through a semiconductor substrate;
aligning at least one bond pad of a semiconductor device with said at least one aperture;
disposing conductive material within said at least one aperture to contact said at least one bond pad.

58. The method of claim 57, wherein said defining said at least one aperture comprises laser drilling.

59. The method of claim 57, wherein said defining said at least one aperture comprises etching.

60. The method of claim 57, wherein said aligning comprises substantially aligning a first periphery of a first wafer including said semiconductor device with a second periphery of a second wafer comprising said semiconductor substrate.

61. The method of claim 60, further comprising singulating said semiconductor device from said first wafer and substantially simultaneously singulating a corresponding portion of said semiconductor substrate from said second wafer.

62. The method of claim 57, further comprising securing said semiconductor device to said semiconductor substrate.

63. The method of claim 62, wherein said securing comprises disposing an adhesive material between said semiconductor device and said semiconductor substrate.

64. The method of claim 62, wherein said securing comprises bonding said conductive material to said at least one bond pad.

65. The method of claim 57, further comprising disposing an insulative material on a surface of said semiconductor substrate.

66. The method of claim 65, wherein said disposing said insulative material comprises growing an oxide on said surface.

67. The method of claim 65, wherein said disposing said insulative material comprises forming an insulative layer on said surface.

68. The method of claim 65, wherein said disposing said insulative material comprises disposing said insulative material on a surface of said semiconductor substrate opposite said semiconductor device.

69. The method of claim 57, further comprising fabricating at least one contact proximate a surface of said semiconductor substrate and in communication with said conductive material.

70. The method of claim 57, further comprising disposing a conductive bump in communication with said conductive material.

71. The method of claim 70, wherein said disposing said conductive bump comprises disposing a solder ball in communication with said conductive material.

72. The method of claim 57, further comprising fabricating a conductive trace extending substantially laterally from said conductive material.